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Ultra Large Scale Manufacturing Challenges of Silicon Carbide and Gallium Nitride Based Power Devices and Systems

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Both silicon carbide (SiC) and gallium nitride (GaN) have the potential of developing transformative power electronics for future needs. The defect density of current devices is quite high and only niche applications will continue to evolve unless major changes are made in the manufacturing process. In this paper we have proposed advanced process control (APC) based single wafer processing (SWP) tools for manufacturing SiC and GaN power devices. New manufacturing tools have the potential of realizing full potential of these materials.

Introduction

Similar to low power electronics, the power electronics based products and systems have relied for many decades on various silicon power semiconductor devices to control and convert electrical power in an efficient and cost-effective manner. Silicon based power metal oxide semiconductor field effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) are the workhorse chips that are used in the manufacturing of power electronic systems. The potential of wide band gap (WBG) semiconductors for manufacturing ultra-high performance power devices and systems is well known (1). Historically, silicon carbide research is as old as is the discovery of transistors (2). About five years ago, some power electronics chipmakers claimed that two WBG technologies based on gallium nitride (GaN) on silicon and silicon carbide (SiC) MOSFETs would displace the ubiquitous silicon power MOSFET [3]. In addition, GaN and SiC based transistors were supposed to pose a threat to higher-end, silicon-based IGBTs (3). However, these predictions did not come to fruition. Other than some niche applications, Si based power MOSFET and IGBT have the major market share at this moment, and may continue to hold the lead for a number of years (3). Power electronics manufacturing companies are still pushing to extract the best from Si based power MOSFET and IGBT (4). In recent years, significant progress has been made in reducing the defect densities of bulk SiC and GaN wafers (5). However, as stated earlier WBG based power systems are commercially available only for some niche applications. The progress is not sufficient to bring the performance, yield and reliability requirements that are warranted for transformative changes in power electronics industry (1).The objective of this paper is to analyze the current SiC and GaN power device results and propose manufacturing changes that should have the potential of large scale commercialization of these devices in power electronics.

Status of Current Silicon Carbide and Gallium Nitride Power Devices and Identification of Major Manufacturing Challenges

Fig. 1 shows the timeline of key events in manufacturing of WBG materials and devices (6). Homoepitaxial growth of SiC allows one to fabricate both vertical and lateral devices. However, heteroepitaxial growth of GaN on either SiC or Si mostly restricts us to lateral devices. Though, it had been asserted that GaN vertical device would deliver superior performance, the cost of bulk GaN substrate is prohibitive for manufacturing and its small wafer size renders it unsuitable for use in state-of-the-art fabs. However, some vertical GaN fabrication attempts were reported on Si substrate (7).

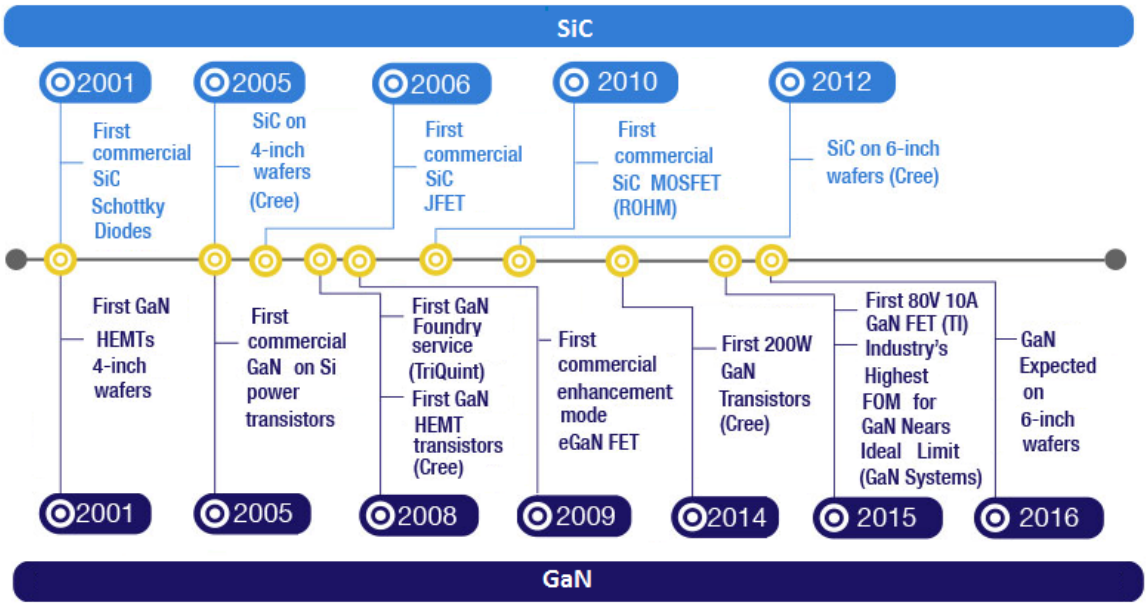

Figure 1: WBG manufacturing timeline with some key products. Adapted from (6).

On the other hand, lateral devices may allow heterogeneous integration i.e. Si based CMOS and GaN based power electronics can be fabricated on same piece of die (8, 9). Fig. 2 (8) shows one such example where Si based p-MOSFET and GaN based HEMT are fabricated on a Si wafer. Innovative approach of chip-scale packaging enhancement-mode GaN field effect transistors has created niche market in low voltage (< 100 V) range (10).

An examination of the literature shows that large defect density (bulk defects in the SiC and GaN wafers as well as process induced defects) is the major barriers in realizing the full potential of these materials for power electronics. It is worth mentioning here that for low voltage applications (e.g. light emitting diodes) these defects may have minimal effect on the device performance and reliability, but at high electric field (e.g. power devices) these defects will have catastrophic impact on the device performance, reliability and electromagnetic interference (EMI). As an example the temperature-dependent turn-on loss in GaN devices has been attributed to decreased trans-conductance (11), which is directly related to defects and temperature controlling the mobility of the GaN material.

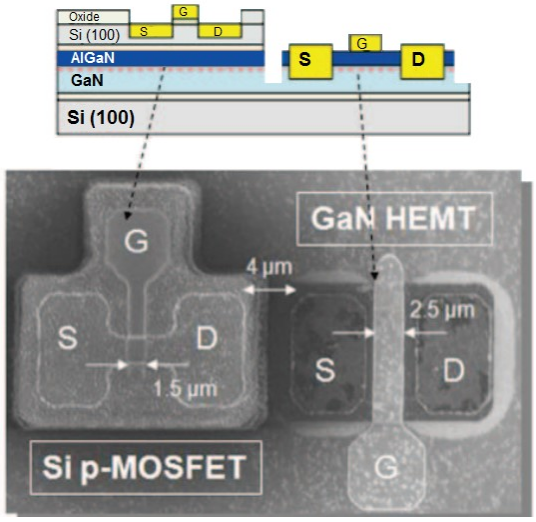

Figure 2: Schematic and SEM image of Si p-MOSFET and GaN HEMT fabricated on Si(100) wafer (8).

A comparative study (12) of commercially available enhancement-mode GaN (e-GaN) devices with those of Si MOSFET devices of the same voltage and current ratings shows that devices show excellent reduction in switching times and switching losses over the Si MOSFET devices, indicating their suitability for high-frequency power conversion. However, as compared to Si devices, the reverse conduction drop and leakage currents are higher with eGaN devices (12). Theoretically, due to higher band gap, the leakage current of GaN devices should be lower than Si devices. These observations can be attributed to defects that are responsible for higher leakage currents.

Table I shows the thickness variation of Si and SiC wafers. The larger percentage variation observed for SiC wafers raises the open question about the control system used in the growth of SiC wafers. However, in this paper we will not discuss the issues related to bulk defects of of SiC and GaN wafers, which we have discussed in previous a publication (4). In the following section, we will present manufacturing scheme that can reduce the process induced defect density of WBG devices.

TABLE I. Thickness Variation of Si and SiC Wafers

Semiconductor	Thickness Variation	% Variation
Si	775 ± 25	3.23 (13)
SiC	350 ± 25	7.14 (14)

Manufacturing Changes for Reducing Densities of WBG Devices

Bringing a commercial product in market and maintaining its profit margin is a mammoth task for any manufacturer. A manufacturer's success is not only measured by the performance of a product, but also through its commercial success and sustaining profitability through these products in the long run. From the prototype and minimum viable product (MVP) to profitable margins, the manufacturer has to consider the market forces and directions. As discussed in the previous section, bulk crystal defects and process induced defects are still the major road blocks in creating a SiC and GaN semiconductor based power electronics. This is due to the fact that best values of

performance, reliability and yield of semiconductor products can be obtained only when the microstructure is homogenous and minimum defect density is observed (15). The defects and process variation are directly related to the yield. From the manufacturing point of view, the loss of yield will can push the cost of ownership (COO) to higher values. The total cost of ownership is given as (16)

$$COO = \frac{CF+CV+CY}{TPT \times Y \times U} \quad [1]$$

where, CF = fixed cost, CV = variable cost, CY = cost due to yield loss,
TPT = throughput, Y = composite yield, and U = utilization.

Part of the success of silicon integrated circuit (IC) industry is due to the fact that in the last 50 years, the defect density (See Fig. 3(17)) of the materials involved in Si IC manufacturing has been reduced by more than four orders of magnitudes. Simplified expression of the yield of integrated circuit is given by

$$Y = e^{-DA} \quad [2]$$

where, D represent the defect density and A is die area. As shown in Fig. 4, (18) the reduction of defect density shown in Fig. 3 has allowed to use larger die size for each generation of technology. The combination of line width reduction, increase of die size and increase of wafer size has allowed to continuously reduce the cost of silicon ICs.

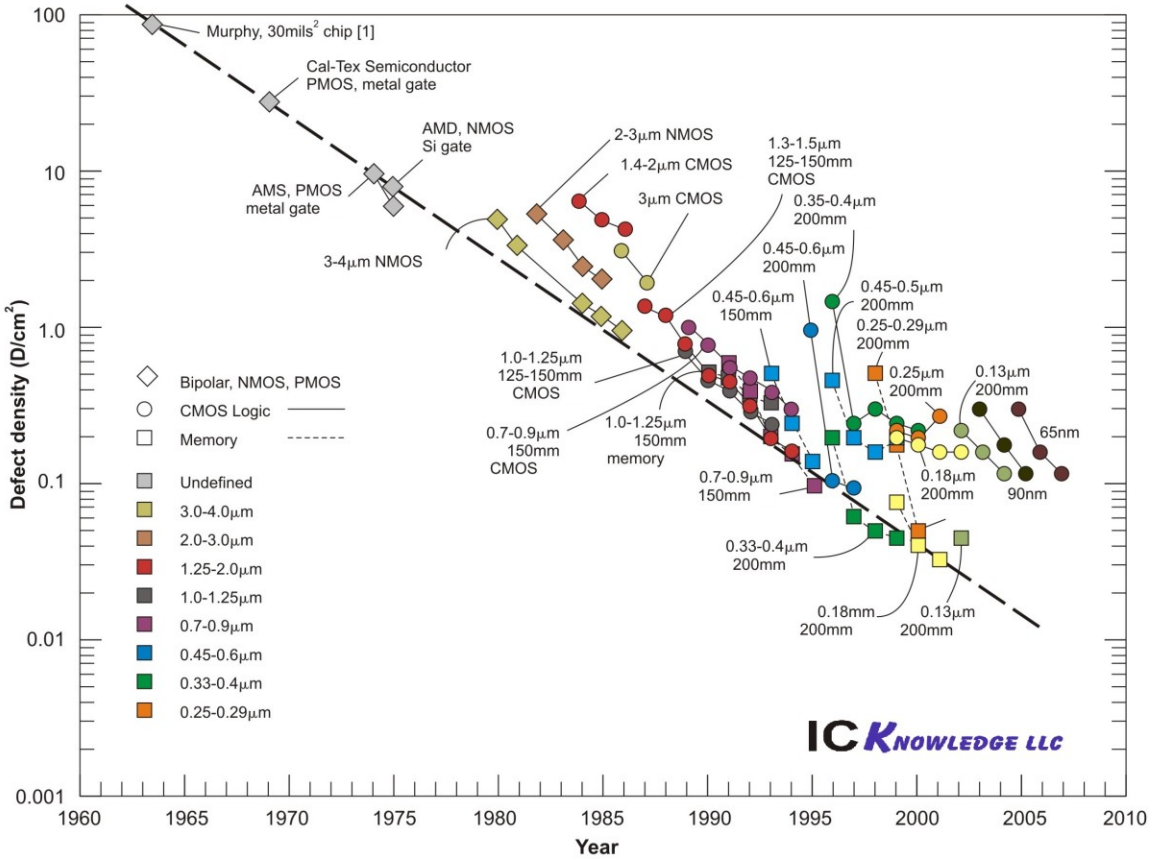

Figure 3: Reduction of defect density over the last 50 years (17). © IC Knowledge LLC.

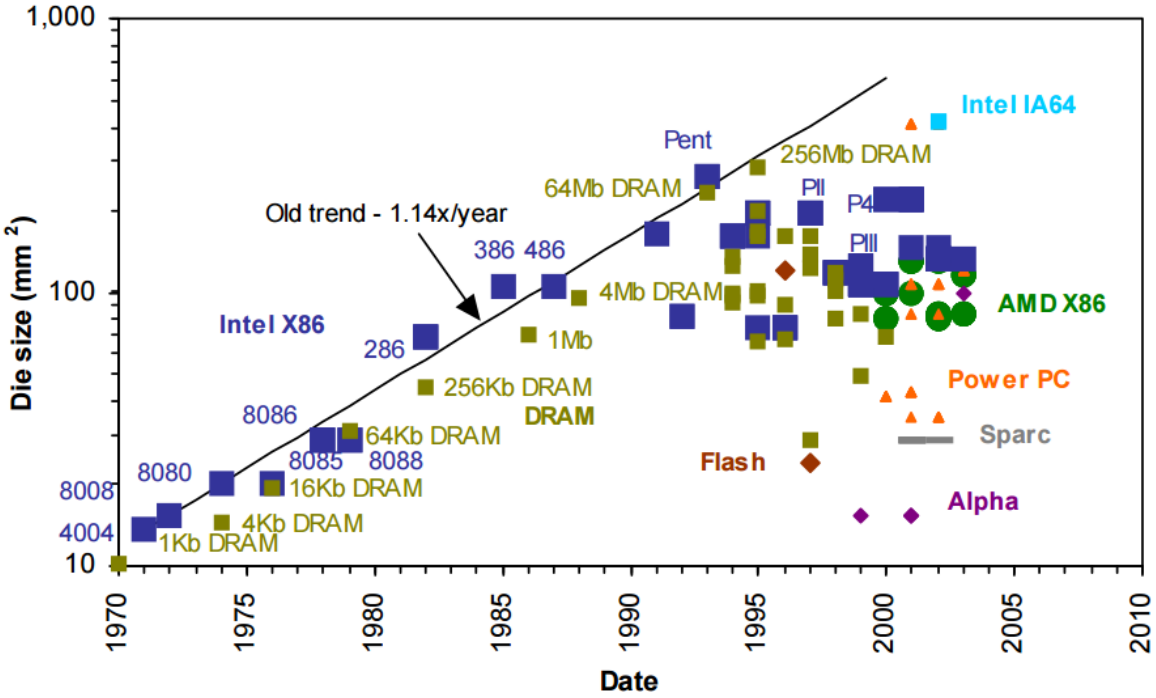

Figure 4: Use of larger die size with progression of time for manufacturing Si ICs (18).

The prime reason for the success of silicon manufacturing is that the process control of semiconductor manufacturing has evolved from classical statistical process control (SPC) to advanced process control (APC). In other words silicon IC industry has virtually adopted single wafer processing (SWP) to address the issue of defect density and other manufacturing considerations (19). The use of advanced process control in SWP allows the control of defect density as well variability of device parameters. In place of conventional thermal processing, rapid thermal processing is used to provide shorter processing time and lower processing temperature resulting in lower defect densities. In addition, the use of high energy incoherent photons in single wafer thermal processing (20) and single wafer chemical vapor deposition (21) provides ultra-high performance, reliable and low-cost devices. The general notion in the WBG semiconductor based power devices and power system community has been that older generation of silicon manufacturing is good enough to manufacturer WBG based power devices (22). This assumption is not true, since unlike silicon the substrate defect density is much higher than the silicon wafers. In case of WBG materials, most of the commercial epitaxial growth systems are also using batch processing (23, 24). Due to high process variability the batch processing tools provide higher defect density and lower yield and lower reliability than corresponding APC controlled SWP tools.

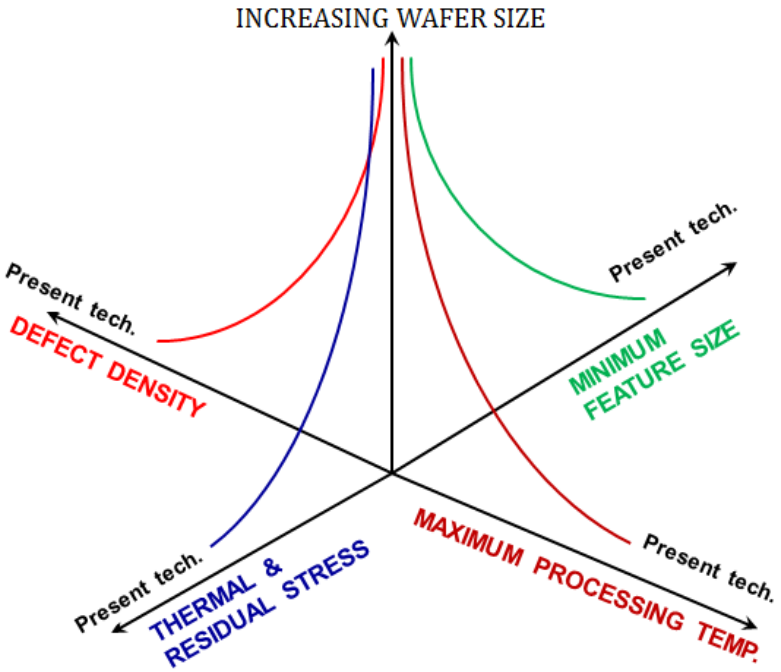

Figure 5: Process integration of WBG devices manufactured by single wafer processing.

Based on the continued success of silicon IC industry, the WBG equipment manufacturers have to develop new processing equipment based on advanced process control. A detailed description of new APC requirements for developing new processing tools is given in reference (24). In Table II, we have summarized the core requirements of new APC based processing tools. From process integration point of view the approach shown in Fig. 5 will lead to devices with reduced defect density. Equipment manufacturers have to develop APC based processing tools that can be used in cluster tool architecture leading to reduced cost of ownership.

TABLE II. Process control fundamentals (25)

Key Issue	Process Control Concerns
Quantifying	Capability to measure is the pre-requisite of controlling something
Locating	The reasons/ origins have to be known before taking a control action
Cost-effectiveness	Over-inspecting is better than inspecting less and taking risk
Change incorporation	It is necessary to quantify the possible losses in worst case
Variability	It is unwanted in process control realm
Reliability	Improved yield has positive impact on reliability
Time	Delay causes loss in throughput and revenue
Late-stage discovery	Problems / defects found later costs and wastes more
Scaling down	Process control requirements increase
Critical problems	May require layered process control strategy
Overall impact	Reduced production cost and cycle time through more process control

Conclusion

In this paper we have examined the current status of SiC and GaN power semiconductor devices. Current practice of the use statistical process control based batch processing leads to larger process variability, and higher defect density leading to lower performance, lower reliability, lower yield and high cost of power devices. Advanced process control based single wafer processing tools are proposed to realize the true potential of SiC and GaN in manufacturing power semiconductor devices.

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